Features

- **n** Customizable power consumption
- **n** Dual LED indicator
- **n** Custom memory maps
- **n** Built in diagnostic functions
- **n** Supports 40Gbps total data rate
- **n** Host-pluggable MSA footprint
- **n** Full SFF-8436 MSA compliant
- **n** Temperature range from 0◦ to 80◦C
- **n** No reference clock required
- **n** Compliant with SONET, SDH, GBE, FC
- **n** MSA Compliant EEPROM

Application

- **n** QSFP Port/System Testing
- **n** ITU-T Recommendation G.957 (STM-1, 4 & 16)
- **n** Ethernet IEEE 802.3 (Gigabit, 10 Gigabit and 40 Gigabit Ethernet)
- **n** SDR, DDR and QDR
- **n** SONET, SDH, GBE, FC Support, Infiniband

Description

This product is a loopback module in a QSFP form factor. The tinout QSFP loopback provides 4 pairs of

transmit data channels connected to the corresponding receive channels. These data channels can operate at transmissions speeds in excess of 10Gbps. In addition, this loopback records the number of cycles/insertions into a powered host and records that value at address 224-225 of the serial ID. This product compliant with the QSFP MSA (SFF 8436). The tinout QSFP loopback provides a cost effective alternative to testing with optical links.
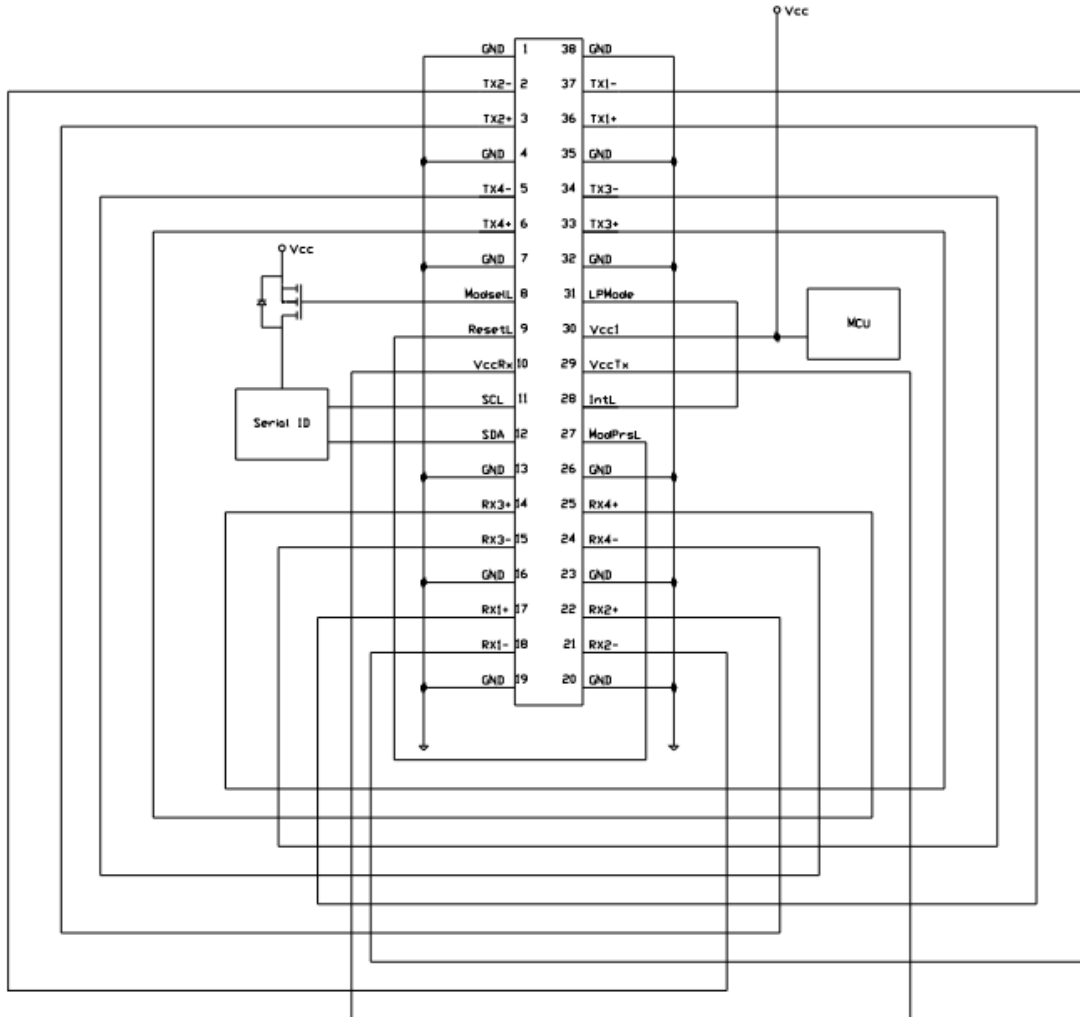

Figure1. Wiring Diagram

Pin Descriptions

Pin	Logic	Symbol	Name/Description
1	/	GND	Module Ground
2	CML-I	Tx2-	Transmitter inverted data input
3	CML-I	Tx2+	Transmitter non-inverted data input
4	/	GND	Module Ground

5	CML-I	Tx4-	Transmitter inverted data input
6	CML-I	Tx4+	Transmitter non-inverted data input
7	/	GND	Module Ground
8	LVTTL-I	MODSEIL	Module Select
9	LVTTL-I	ResetL	Module Reset
10	/	VCCRx	+3.3v Receiver Power Supply
11	LVCMOS-I	SCL	2-wire Serial interface clock
12	LVCMOS-I/O	SDA	2-wire Serial interface data
13	/	GND	Module Ground
14	CML-O	RX3+	Receiver non-inverted data output
15	CML-O	RX3-	Receiver inverted data output
16	/	GND	Module Ground
17	CML-O	RX1+	Receiver non-inverted data output
18	CML-O	RX1-	Receiver inverted data output
19	/	GND	Module Ground
20	/	GND	Module Ground
21	CML-O	RX2-	Receiver inverted data output
22	CML-O	RX2+	Receiver non-inverted data output
23	/	GND	Module Ground
24	CML-O	RX4-	Receiver inverted data output
25	CML-O	RX4+	Receiver non-inverted data output
26	/	GND	Module Ground
27	CML-O	ModPrsL	Module Present, internal pulled down to GND
28	CML-O	IntL	Interrupt output, should be pulled up on host board
29	/	VCCTx	+3.3v Transmitter Power Supply
30	/	VCC1	+3.3v Power Supply
31	LVTTL-	LPMode	Low Power Mode
32	/	GND	Module Ground
33	CML-I	Tx3+	Transmitter non-inverted data input
34	CML-I	Tx3-	Transmitter inverted data input
35	/	GND	Module Ground
36	CML-I	Tx1+	Transmitter non-inverted data input
37	CML-I	Tx1-	Transmitter inverted data input
38		GND	Module Ground

Notes:

TINOUT TECHNOLOGY LIMITED

1. GND is the symbol for signal and supply (power) common for the QSFP module. All are
common within the QSFP module and all module voltages are referenced to this potential unless otherwise noted.
Connect these directly to the host board signal-common ground plane

2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Vcc Rx, Vcc1and Vcc Tx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for a maximum current of 500 mA.

Top Side Viewed from Top		Bottom Side Viewed from Bottom	
38	GND	GND	1
37	TX1n	TX2n	2
36	TX1p	TX2p	3
35	GND	GND	4
34	TX3n	TX4n	5
33	TX3p	TX4p	6
32	GND	GND	7
31	LPMode	ModSelL	8
30	Vcc1	ResetL	9
29	VccTx	VccRx	10
28	IntL	SCL	11
27	ModPrsL	SDA	12
26	GND	GND	13
25	RX4p	RX3p	14
24	RX4n	RX3n	15
23	GND	GND	16
22	RX2p	RX1p	17
21	RX2n	RX1n	18
20	GND	GND	19

Card Edge

Top Side
Viewed from Top

Bottom Side
Viewed from Bottom