FEATURES

- XAUI Electrical Interface: 4 Lanes @ 3.125Gbit/s
- Hot Z-Pluggable
- SC-Duplex Optical Receptacle
- MDIO, DOM Support
- Cooled 1.3μm DFB-LD
- PIN Photo-detector
- Operating Case Temperature: 0 to 70 °C
- Compliant to IEEE 802.3ae 10GBASE-LR Application
- Compliant to XENPAK MSA
- Mechanical Footprint: 4.76" L x 1.42" W x 0.46" H

REFERENCE

- IEEE 802.3ae as 10GBASE-ER, XENPAK MSA Release3.0

DESCRIPTION

- **General**

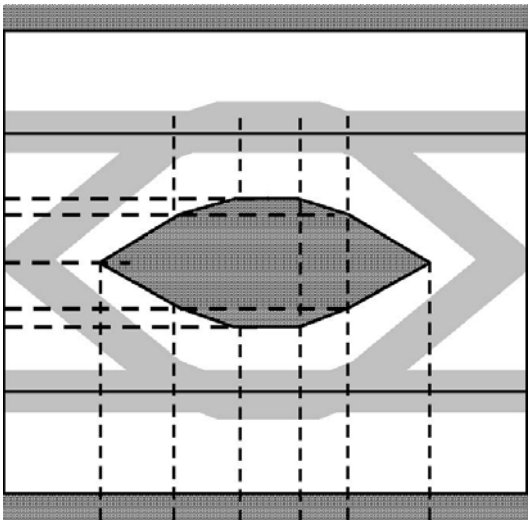
POFLink's 10GbE XENPAK transceiver module PLK-10GB-LR is a hot pluggable in the Z-direction module that is usable in typical router line card applications, Storage, IP network and LAN and compliant to XENPAK MSA. The PLK-10GB-LR is a fully integrated 10.3Gbit/s optical transceiver module that consists of a 10.3Gbit/s optical transmitter and receiver, XAUI interface, Mux and Demux with clock and data recovery(CDR). This version of POFLINK Inc. transceiver line uses an cooled 1310nm DFB Laser Diode to achieve 10km over standard single mode fiber as 10GBASE-LR of the IEEE 802.3ae.

PERFORMANCE SPECIFICATIONS

Optical Characteristics

Table 1. Optical Characteristics

No.	Parameters	Symbols	Min.	Typ.	Max.	Unit	Remarks
1	Center Wavelength	λ_C	1290	1310	1330	nm	
2	Signaling speed		-	10.3125	-	Gbit/s	
3	Signaling speed variation from nominal		-100	-	+100	ppm	
4	Optical modulation amplitude	OMA	-5.2	-	-	dBm	Note 1
5	Optical Output Power	P_f	-5	-	0	dBm	Average
6	Optical Waveform	-				-	
7	Side Mode Suppression Ratio	S_r	30	-	-	dB	Average
8	Extinction Ratio	E_r	3.5	-	-	dB	
9	Off Transmit Power	P_{off}	-	-	-30	dBm	Average
10	Optical Output turn-off Time	T_{TX-OFF}	-	-	100	μs	Figure10
11	Receiver Sensitivity in OMA	OMArmin	-21	-	-7	dBm	
12	Receiver Overload	R_{ro}	+0.5	-	-	dBm	Average
13	Receiver Return Loss	R_L	12	-	-	dB	Average



Electrical Performance

Table2. Power Supply Characteristics

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
1	Supply Voltage	V_{CC1}	3.135	3.300	3.465	V	
2	Supply Voltage	V_{CC2}	1.152	1.200	1.248	V	
3	Supply Current	I_{CC1}	-	-	1.4	A	+3.3 V
4	Supply Current	I_{CC2}	-	-	1.7	A	APS
5	Power Consumption	P_{DS}	-	-	3.0	W	
6	Power supply stabilization time	T_{DF}	-	-	500	ms	Figure 7
7	Initialization Time	T_{INIT}	-	-	5	s	Figure 7
8	RESET Assert Time	T_{RESET}	1	-	-	ms	Figure 9
9	Hold Time after rising edge of RESET	T_{HOLD}	500	-	-	ms	Figure 9

Table 3. XAUI Driver Characteristics

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
1	Baud Rate		-	3.125	-	Gbit/s	
2	Baud Rate Tolerance		-100	-	+10	ppm	

					0		
3	Differential Amplitude		800	-	1600	mV_{PP}	AC, near-end value

Table4. 1.2VCMOS Interface Characteristics

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
1	Baud Rate		-	3.125	-	Gbit/s	
2	Baud Rate Tolerance		-100	-	+100	ppm	
3	Differential Amplitude		200	-	1600	mVpp	AC

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
1	Input High Voltage	V_{IH}	0.84	-	1.5	V	
2	Input Low Voltage	V_{IL}	-0.3	-	0.36	V	
3	Input Pull-down Current	I_{In}	20	40	120	μA	Vih=1.2V
4	Output High Voltage	V_{OH}	1.0	-	-	V	Pull-up=10k ohm to 1.2V
5	Output Low Voltage	V_{OL}	-	-	0.2	V	
6	Pull up Resistance	R_{LASI}	10	-	22	k ohm	Figure 8
7	Capacitance	C_{LASI}	-	-	10	pF	Figure 8
8	Load Capacitance	C_{Load}	-	-	320	pF	Figure 8

Table5. MDIO Bidirectional Interface Characteristics

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
1	Input High Voltage	V_{IHM}	0.84	-	1.5	V	
2	Input Low Voltage	V_{ILM}	-0.3	-	0.36	V	
3	Output High Voltage	V_{OHM}	1.0	-	1.5	V	
4	Output Low Voltage	V_{OLM}	-0.3	-	0.2	V	
5	Pull up Resistance	R_{MDIO}	200	-	Note 1	Ohm	Figure 5
6	MDC min high/low time	T_{HM},T_{LM}	160	-	-	ns	Figure 3

7	MDC Frequency	1/T_{CK}	TBD	-	2.5	MHz	
8	Setup time	T_{DIS}	10	-	-	ns	Figure 3
9	Hold time	T_{DIH}	10	-	-	ns	Figure 3
10	MDIO output delay after rising edge of MDC	T_{PD}	0	-	300	ns	Figure 4
11	Input Capacitance	Ci	-	-	10	pF	Figure 5
12	Bus Loading	CL			470	pF	Figure 5

Note 1 : The maximum value of R_{MDIO} depends on bus loading(C_L) , input capacitance(Ci), and MDC frequency(1/T_{CK}).

70	GND	1	GND
69	GND	2	GND
68	RESERVED	3	GND
67	RESERVED	4	RESERVED
66	GND	5	3.3V
65	TX LANE3	6	3.3V
64	TX LANE3+	7	APS
63	GND	8	APS
62	TX LANE2	9	LASI
61	TX LANE2+	10	RESET
60	GND	11	VEND SPECIFIC
59	TX LANE1	12	TX ON/OFF
58	TX LANE1+	13	RESERVED
57	GND	14	MOD DETECT
56	TX LANE0	15	VEND SPECIFIC
55	TX LANE0+	16	VEND SPECIFIC
54	GND	17	MDIO
53	GND	18	MDC
52	GND	19	PRTAD4
51	RX LANE3	20	PRTAD3
50	RX LANE3+	21	PRTAD2
49	GND	22	PRTAD1
48	RX LANE2	23	PRTAD0
47	RX LANE2+	24	VEND SPECIFIC
46	GND	25	APS SET
45	RX LANE1	26	RESERVED
44	RX LANE1+	27	APS SENSE
43	GND	28	APS
42	RX LANE0	29	APS
41	RX LANE0+	30	3.3V

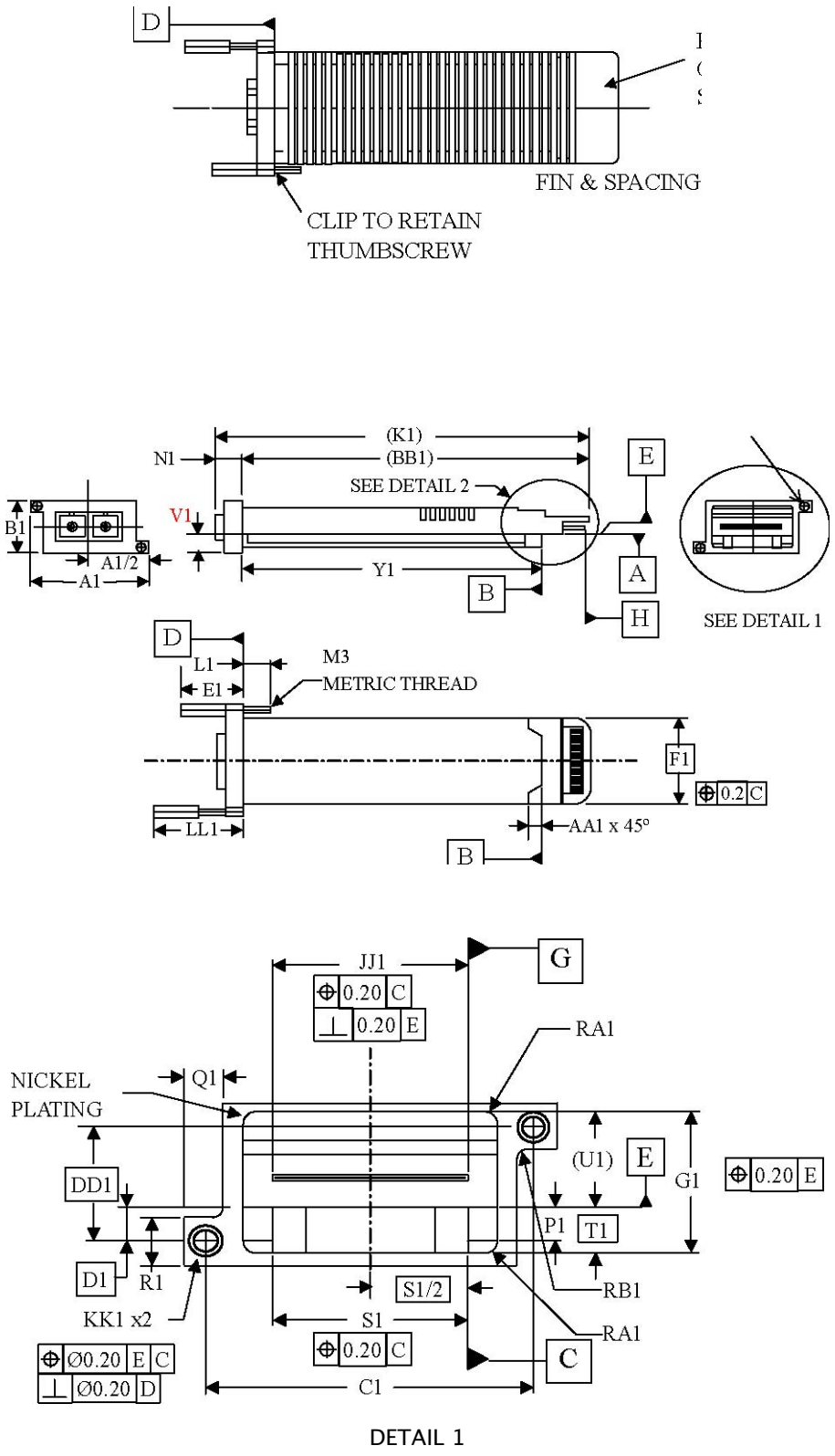
40	GND	31	3.3V
39	RESERVED	32	RESERVED
38	RESERVED	33	GND
37	GND	34	GND
36	GND	35	GND

Figure 1 XENPAK Pin Configuration Figure 2 Mechanical dimensions Refer to Table 10 for Dimensions

Pin #	Symbol	I/O	Logic	Description	Notes
1	GND	I	Supply	Electrical ground	
2	GND	I	Supply	Electrical ground	
3	GND	I	Supply	Electrical ground	
4	RESERVED	-	-	Reserved	
5	3.3 V	I	Supply	Power	
6	3.3 V	I	Supply	Power	
7	APS	I	Supply	Adaptive Power Supply	
8	APS	I	Supply	Adaptive Power Supply	
9	LASI	O	Open Drain	Link Alarm Status Interrupt. 10-22k ohm pull up on host.	
10	RESET	I	1.2V CMOS	TX OFF when MDIO RESET	
11	VEND SPECIFIC	-	-	Vendor Specific Pin. Leave unconnected.	
12	TX ON/OFF	I	1.2V CMOS	Transmitter ON/OFF	
13	RESERVED	-	-	Reserved	
14	MOD DETECT	O	-	Pulled low inside module through 1k ohm.	
15	VEND SPECIFIC	-	-	Vendor Specific Pin. Leave unconnected.	
16	VEND SPECIFIC	-	-	Vendor Specific Pin. Leave unconnected.	
17	MDIO	I/O	Open Drain	Management Data IO	
18	MDC	I	1.2V CMOS	Management Data Clock	
19	PRTAD4	I	1.2V	Port Address bit 4	

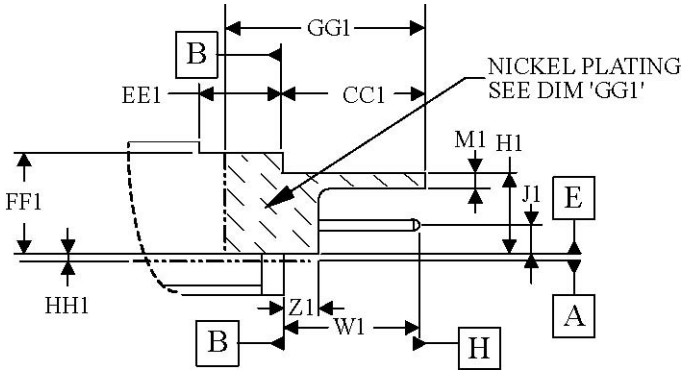
			CMOS	(Low=0)	
20	PRTAD3	I	1.2V CMOS	Port Address bit 3 (Low=0)	
21	PRTAD2	I	1.2V CMOS	Port Address bit 2 (Low=0)	
22	PRTAD1	I	1.2V CMOS	Port Address bit 1 (Low=0)	
23	PRTAD0	I	1.2V CMOS	Port Address bit 0 (Low=0)	
24	VEND SPECIFIC	-	-	Vendor Specific Pin. Leave unconnected.	
25	APS SET	O	-	Feedback output for APS	
26	RESERVED	-	-	Reserved for Avalanche Photodiode use.	
27	APS SENSE	O	Analog	APS Sense Connection	
28	APS	I	Supply	Adaptive Power Supply	
29	APS	I	Supply	Adaptive Power Supply	
30	3.3 V	I	Supply	Power	
31	3.3 V	I	Supply	Power	
32	RESERVED	-	-	Reserved	
33	GND	I	Supply	Electrical Ground	
34	GND	I	Supply	Electrical Ground	
35	GND	I	Supply	Electrical Ground	
36	GND	I	Supply	Electrical Ground	
37	GND	I	Supply	Electrical Ground	
38	RESERVED	-	-	Reserved	
39	RESERVED	-	-	Reserved	
40	GND	I	Supply	Electrical Ground	
41	RX LANE 0+	O	AC	Module XAUI Output Lane 0+	
42	RX LANE 0-	O	AC	Module XAUI Output Lane 0-	
43	GND	I	Supply	Electrical Ground	
44	RX LANE 1+	O	AC	Module XAUI Output Lane 1+	
45	RX LANE 1-	O	AC	Module XAUI Output Lane 1-	
46	GND	I	Supply	Electrical Ground	
47	RX LANE 2+	O	AC	Module XAUI Output Lane	

				2+	
48	RX LANE 2-	O	AC	Module XAUI Output Lane 2-	
49	GND	I	Supply	Electrical Ground	
50	RX LANE 3+	O	AC	Module XAUI Output Lane 3+	
51	RX LANE 3-	O	AC	Module XAUI Output Lane 3-	
52	GND	I	Supply	Electrical Ground	
53	GND	I	Supply	Electrical Ground	
54	GND	I	Supply	Electrical Ground	
55	TX LANE 0+	I	AC	Module XAUI Input Lane 0+	
56	TX LANE 0-	I	AC	Module XAUI Input Lane 0-	
57	GND	I	Supply	Electrical Ground	
58	TX LANE 1+	I	AC	Module XAUI Input Lane 1+	
59	TX LANE 1-	I	AC	Module XAUI Input Lane 1-	
60	GND	I	Supply	Electrical Ground	
61	TX LANE 2+	I	AC	Module XAUI Input Lane 2+	
62	TX LANE 2-	I	AC	Module XAUI Input Lane 2-	
63	GND	I	Supply	Electrical Ground	
64	TX LANE 3+	I	AC	Module XAUI Input Lane 3+	
65	TX LANE 3-	I	AC	Module XAUI Input Lane 3-	
66	GND	I	Supply	Electrical Ground	
67	RESERVED	-	-	Reserved	
68	RESERVED	-	-	Reserved	
69	GND	I	Supply	Electrical Ground	
70	GND	I	Supply	Electrical Ground	



DETAIL 1

Figure 3 Mechanical dimensions of End View of Transceiver



DETAIL 2

Figure4 Mechanical dimensions of Side Elevation Transceiver

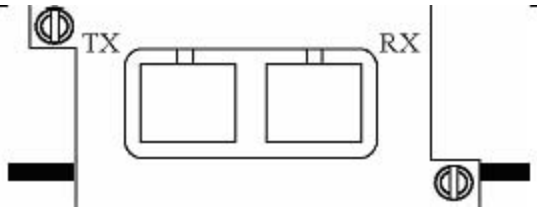


Figure 5 Orientation Keying of TX and RX Orientation Vs PCB Table 7 Package

Dimensions Table11 Definition of Datum

KEY	VALUE, mm / inch	TOLERANCE mm	COMMENTS
A1	51.3 2.020	±0.20	Width of Bezel overall
B1	22.4 0.882	±0.20	Height of Bezel overall
C1	45.5 1.791	BASIC	Distance between captive screws in 'X' axis (Horizontal)
D1	3.7 0.136	BASIC	Datum 'E' to lower captive screw
E1	20.75 0.817	Maximum	Extension of captive screw
F1	36.0 1.417	±0.20	Width of Transceiver body
G1	17.4 0.685	±0.20	Height of Transceiver body
H1	8.15 0.321	±0.20	Datum 'E' to top of Over-hanging Ledge
J1	3.05 0.120	±0.25	Datum 'E' to centerline of Transceiver PCB
K1	(121.0) 4.764	REF	Length of Transceiver overall minus protruding captive screw heads
L1	5.00 0.197	±0.20	Length of captive screw from Datum 'D' to end of threaded end

M1	1.5 0.059	±0.20	Thickness of Over-hanging Ledge
N1	5.8 0.228	±0.20	Datum 'D' to front of Transceiver Bezel
P1	4.07 0.160	Minimum	Slot or channel formed by Interposer to accommodate Customers PCB range. Use of an Interposer spring is not a requirement of this specification.
Q1	4.65 0.183	±0.20	Protrusion of side flange on Transceiver Bezel
R1	7.12 0.280	±0.20	Height of side flange on Transceiver Bezel
S1	29.5 1.161	±0.20	Width of Transceiver slot to accommodate rail or Customers PCB
T1	5.42 0.213	BASIC	Datum 'E' to bottom of Transceiver
U1	(11.98) 0.472	REF	Datum 'E' to top of Transceiver
V1	7.92 0.312	±0.20	Datum 'E' to bottom of Transceiver Bezel
W1	11.10 0.437	±0.20	Datum 'B' to end of protruding Transceiver PCB
Y1	102.20 4.024	±0.20	Datum 'D' to Datum 'B'
Z1	4.0 0.157	±0.20	Datum 'B' to end of side protective shroud to mate with EMI/Conn. Shield
AA1	3.0 0.118	±0.50	Datum 'B' to end of 45° chamfer
BB1	(115.2) 4.535	REF	Length of Module from Datum 'D' to rear Over-hanging Ledge
CC1	13.0 0.512	±0.50	Datum 'B' to end of Over-hanging Ledge for EMI Plating
DD1	13.96 0.550	BASIC	Distance between captive screws in 'Y' axis (Vertical)
EE1	10.0 0.394	Minimum	Datum 'B' end of recess for insertion clearance
FF1	10.48 0.422	±0.50	Datum 'E' to top of recess for insertion clearance
GG1	20.0 0.787	Minimum	Length of Transceiver side wall for EMI plating
HH1	0.25 0.01	BASIC	Datum 'A' to Datum 'E'
JJ1	29.2 1.150	±0.10	Width of Transceiver PCB
KK1	3.0 0.118	N/A	Hole for 3mm screw Thumbscrew, tapped or clearance
LL1	25.8 1.016	Maximum	Length of Thumbscrew
RA1	1.25 0.049	Minimum	External radius or chamfer of

			Transceiver
RB1	1.5 0.059	Maximum	Internal radius or chamfer on exterior flange of Transceiver Bezel

DATUM	DESCRIPTION TRANSCEIVER/LINECARD
A	CUSTOMERS PCB TOP SURFACE
B	PHYSICAL HARD STOP FOR TRANSCEIVER
C	EDGE OF TRANSCEIVER SLOT
D	BACK SURFACE OF TRANSCEIVER BEZEL, SAFETY HARD STOP
E	TRANSCEIVER TOP SURFACE OF SLOT 'P1'
F	FRONT SURFACE OF CUSTOMERS FACEPLATE
G	EDGE OF TRANSCEIVER'S PCB
H	LEADING EDGE OF TRANSCEIVER PCB
J	EDGE OF CUT-OUT IN CUSTOMER'S PCB
K	PHYSICAL HARD STOP ON CUSTOMER'S PCB

Optical Connector

No.	Parameter	Specifications	Remarks
1	SC Duplex Receptacle	IEC61754-4	Optical bores 12.25/13.15mm
2	SC Duplex plug	IEC61754-4	Optical bores 12.25/13.15mm

Register Definition

Device Address (Dec) Register Address (Hex)	PMA/PMD 1	PCS 3	PHY XS 4
0x0000	PMA/PMD Control1	PCS Control1	PHY XS Control1
0x0001	PMA/PMD Status1	PCS Status1	PHY XS Status1
0x0002	PMA/PMD Device Identifier0	PCS Device Identifier0	PHY XS Device Identifier0
0x0003	PMA/PMD Device Identifier1	PCS Device Identifier1	PHY XS Device Identifier1
0x0004	PMA/PMD Speed Ability	PCS Speed Ability	PHY XS Speed Ability
0x0005	PMA/PMD Device in Package1	PCS Device in Package1	PHY XS Device in Package1
0x0006	PMA/PMD Device in Package2	PCS Device in Package2	PHY XS Device in

			Package2
0x0007	10G PMA/PMD Control2	PCS Control2	Reserved
0x0008	10G PMA/PMD Status2	PCS Status2	PHY XS Status2
0x0009	10G PMD Transmit Disable	Reserved	Reserved
0x000A	10G PMD Receive Signal O.K.	Reserved	Reserved
0x000E	Package Identifier0	Reserved	Reserved
0x000F	Package Identifier1	Reserved	Reserved
0x0018	Reserved	Reserved	10G PHY XGXS Lane Status
0x0019	Reserved	Reserved	10G PHY XGXS Test Control
0x0020	Reserved	10GBASE-R PCS Status1	Reserved
0x0021	Reserved	10GBASE-R PCS Status2	Reserved
0x0022	Reserved	10GBASE-R PCS Test pattern Seed A0	Reserved
0x0023	Reserved	10GBASE-R PCS Test pattern Seed A1	Reserved
0x0024	Reserved	10GBASE-R PCS Test pattern Seed A2	Reserved
0x0025	Reserved	10GBASE-R PCS Test pattern Seed A3	Reserved
0x0026	Reserved	10GBASE-R PCS Test pattern Seed B0	Reserved
0x0027	Reserved	10GBASE-R PCS Test pattern Seed B1	Reserved
0x0028	Reserved	10GBASE-R PCS Test pattern Seed B2	Reserved
0x0029	Reserved Reserved	10GBASE-R PCS Test pattern Seed B3	Reserved
0x002A	Reserved	10GBASE-R PCS Test pattern Control	Reserved
0x002B	Reserved	10GBASE-R PCS Test pattern Error counter	Reserved
0x8000	NVR Control/Status (XENPAK Register)	Reserved	
0x8007 - 0x807D	NVR (XENPAK Register)	Reserved	
0x807E- 0x80AD	Customer AREA	Reserved	
0x80AE - 0x8106	POFLINK Specific Area(XENPAK Register)	Reserved	
0x9000	RX_ALARM Control (XENPAK Register)	Reserved	

0x9001	TX_ALARM Control (XENPAK Register)	Reserved
0x9002	LASI Control (XENPAK Register)	Reserved
0x9003	RX_ALARM Status (XENPAK Register)	Reserved
0x9004	TX_ALARM Status (XENPAK Register)	Reserved
0x9005	LASI Status (XENPAK Register)	Reserved
0x9006	TX_FLAG Control Bits	Reserved
0x9007	RX_FLAG Control Bits	Reserved
0xA000 – 0xA027	Alarm and Warning Thresholds	Reserved
0xA060 – 0xA069	Digital Optical Monitoring Interface	Reserved
0xA06F	DOM Capability – Extended	Reserved
0xA070	TX_ALARM_FLAG Bits	Reserved
0xA071	RX_ALARM_FLAG Bits	Reserved
0xA074	TX_WARNING_FLAG Bits	Reserved
0xA075	RX_WARNING_FLAG Bits	Reserved
0xA100	Optional Digital Optical Monitoring (DOM) Control/Status	Reserved